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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,759	02/20/2004	Takaaki Higashida	2004-0276	3778

513 7590 06/30/2005

WENDEROTH, LIND & PONACK, L.L.P.
2033 K STREET N. W.
SUITE 800
WASHINGTON, DC 20006-1021

EXAMINER	
NGUYEN, DONGHAI D	

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,759	HIGASHIDA ET AL.	
	Examiner	Art Unit	
	Donghai D. Nguyen	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8 and 10-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-8,10 and 11* is/are allowed.

6)☒ Claim(s) *2-5 and 12-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/890,009.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 16 and 17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In this application, the limitation recited: "... to interconnect all ends of the conductive members at the semiconductor ... the base element" (see claim 16, lines 3-6) was not described in the specification in such away to show one skilled in the art that the inventors has possession of the claimed invention.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 16-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation recited in claim 16, lines 1-6 is not understood for the following reasons: It is not known how the forming wiring pattern and the interconnects all ends of the conductive members at the semiconductor element-mounting face of the base member and at the circuit board-mounting face of the base member can be done and how the formed pattern on the

semiconductor element-mounting face being connectively attached to the conductive members and/or circuit board as to form a working device.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 2, 12-14, and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by JP Publication 04-240,759 to Dotani.

Regarding claims 2, 12, and 18, Dotani discloses a method for manufacturing a semiconductor element-mounting board, comprising: arranging a plurality of conductive members (1) in a mold (23); and injecting the resin material (11/21) into the mold after the conductive members are arranging therein so that the conductive members ands the resin material are integrally molded to form a base member (Figs. 1 and 5C) having a semiconductor element-mounting face and a circuit board-mounting face opposite the semiconductor element-mounting face (Fig. 5C), the arranging of the conductive members comprising orienting the conductive members in the mold so that the conductive members are substantially orthogonal to the semiconductor element-mounting face and the circuit board-mounting face and extend linearly through an interior of the base member between the semiconductor element-mounting face and the circuit board-mounting face (Fig. 5A); forming a wiring pattern (13) on the semiconductor surface and on the circuit board surface of the base member so that the wiring

pattern (13) is electrically connected to each end of each of the conductive members (See Figs. 2 or 5D); then, mounting and electrically connecting a semiconductor element (15A) to the semiconductor element-mounting face by a flip-chip mounting process; and then mounting and electrically connecting the circuit board-mounting face to a circuit board (15B in Figs. 4).

Regarding claims 13 and 14, Dotani shows the base member (Fig. 5A) being cut in direction orthogonal to the longitudinal axis of the conductive members (20, see Figs. 5B) to form a desired base member (1, see Fig. 5C).

Regarding claims 16-17 Dotani's Figs. 4-5 shows the IC device (15A) by process of forming conductive pattern face of the PCB and interconnecting the pattern of semiconductor device to the pattern as provided on PCB (15B) to form a device as shown in Fig. 7.

7. Claims 2-4, 12-14, and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by US Pat. 5,364,276 to Inasaka

Regarding claims 2, 12, and 18, Inasaka discloses a method for manufacturing a semiconductor element-mounting board (5), comprising: arranging a plurality of conductive members (1) in a mold (Col. 5, line 69 to Col. 6, line 1)); and injecting the resin material (4, 14, see Col. 4, lines 1-2) into the mold after the conductive members are arranging therein so that the conductive members ands the resin material are integrally molded to form a base member (5, See Figs. 15-16) having a semiconductor element-mounting face (top surface) and a circuit board-mounting face opposite the semiconductor element-mounting face (bottom surface in Fig. 5), the arranging of the conductive members comprising orienting the conductive members in the mold so that the conductive members are substantially orthogonal to the semiconductor element-

mounting face and the circuit board-mounting face and extend linearly through an interior of the base member between the semiconductor element-mounting face and the circuit board-mounting face (Fig. 5); forming a wiring pattern (6/7) on the semiconductor surface and on the circuit board surface of the base member so that the wiring pattern is electrically connected to each end of each of the conductive members (1); then mounting and electrically connecting a semiconductor element (8) to the semiconductor element-mounting face by flip-chip mounting to the wiring pattern formed on the semiconductor element-mounting surface; and mounting and electrically connecting the wiring pattern on the circuit board-mounting face to a circuit board (9, see Fig. 7).

Regarding claims 3 and 4, Inasaka discloses the step of forming the wiring pattern (6/7) see Col. 4, lines 8-11 and 34-55.

Regarding claims 13 and 14, Inasaka discloses a method of manufacturing a semiconductor element-mounting board as described in claim 1 above; further Inasaka discloses the step of cutting at least one of the semiconductor element-mounting face and the circuit board-mounting face after injecting (see Abstract, lines 13-15).

Regarding claim 16-17 as best understood, Inasaka discloses a wiring (6/7) on the semiconductor element-mounting face and the circuit board-mounting face as to connect all ends of the conductive members (1, see Figs. 5-6).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dotani in view of JP Publication No 61-237,458 to Furukawa et al.

Dotani discloses every aspect limitations of the present invention with the exception of roughing or applying adhesive agent to the circumferential surface of the conductor members. Furukawa et al teach the roughing and applying adhesive agent to the circumferential surface of the conductor members for increasing adhesive strength between conductor members and resin (refer to sections of Purpose and Constitution). It would have been obvious to on have ordinary skill in the art at the time the invention was made to modify Dotani's invention by providing the teaching of roughing and applying adhesive agent to the circumferential surface of the conductor members as taught by Furukawa et al as so to provide an increasing adhesive strength and sealing and bonding between conductor members and resin thereof.

Allowable Subject Matter

10. Claims 6-8 and 10-11 are allowed.

Response to Arguments

11. Applicant's arguments with respect to claims 2-5 and 12-18 have been considered but are moot in view of the new ground(s) of rejection.

12. Applicant's arguments filed April 18, 2005 have been fully considered but they are not persuasive. Applicants argue that the metal material (13) of Dotani does not constitute a wiring

pattern as recited in claim 2 (See, "Remarks", page 11, 3rd paragraph). The Examiner disagrees since Dotani discloses the metal material, "wiring pattern", (13) forms on each of semiconductor and circuit element-mounting faces of the base (11) that electrically connected to each end of the conductive members (1) as shown in Figs. 2 and 5D. Therefore, Dotani meets all the limitations cited in claim 2.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghai D. Nguyen whose telephone number is (571)-272-4566. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter D. Vo can be reached on (571)-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DN
June 21, 2005

MINH TRINH
PRIMARY EXAMINER